WHAT IS CLAIMED IS:

1. A semiconductor device, comprising:

a first transistor including a source region, a drain region provided in the same device region as the source region, and a loop-shaped gate electrode region; and

a second transistor sharing, with the first transistor, the loop-shaped gate electrode region and the source region or the drain region.

2. A semiconductor device, comprising:

a device region where each of a plurality of source regions and each of a plurality of drain regions of transistors are alternately included; and

a plurality of loop-shaped gate electrode regions of the transistors which are formed on the device region and part of which are disposed onto two positions between the source regions and the drain regions.

3. A semiconductor device, comprising:

a first device region including a plurality of source regions and a plurality of drain regions of first conductivity type transistors;

a plurality of loop-shaped gate electrode regions of the fist conductivity type transistors, the gate electrode regions being formed on the first device region;

a second device region including a plurality of source regions and a plurality of drain regions of second conductivity

type transistors;

a plurality of loop-shaped gate electrode regions of the second conductivity type transistors, each of the gate electrode regions being formed on the second device region and electrically coupled to each of the gate electrode regions of the first conductivity type transistors;

a first wiring configured to supply a first voltage to at least one of the source regions of the first device region;

a second wiring configured to supply a second voltage to at least one of the source regions of the second device region; and

a third wiring electrically coupled to the drain regions of the first and second device regions and to the gate electrode regions of the first and second conductivity type transistors.

4. The semiconductor device of claim 1, wherein the drain region is formed in a region surrounded by the loop-shaped gate electrode region.

5. The semiconductor device of claim 1, wherein an electrically independent drain region is formed in a region surrounded by the loop-shaped electrode region.

6. The semiconductor device of claim 1, wherein the source region is formed outside a region surrounded by the loop-shaped gate electrode region.

7. The semiconductor device of claim 1, wherein a plurality of the source regions are formed outside a region surrounded by the loop-shaped gate electrode region, the

plurality of the source regions electrically coupled to each other.

8. The semiconductor device of claim 1, wherein the respective loop-shaped gate electrode regions have same lengths on the device region and a device isolation region except contact regions between wiring portions and the gate electrode regions.

9. The semiconductor device of claim 1, wherein the semiconductor device includes a fourth wiring electrically coupled to the gate electrode regions of the first and second conductivity type transistors, the fourth wiring has at least two connection portions to the gate electrode regions.

10. The semiconductor device of claim 9, wherein the fourth wiring is disposed above the drain region.

11. The semiconductor device of claim 10, wherein the gate electrode regions of the first and second conductivity type transistors are coupled by a wiring.

12. The semiconductor device of claim 10, wherein the gate electrode regions of the first and second conductivity type transistors are coupled by a region made of a material to form the gate electrode regions.

13. The semiconductor device of claim 3, wherein a shape of the gate electrode region of the first conductivity type transistor is different from that of the gate electrode region of the second conductivity type transistor.

14. The semiconductor device of claim 3, wherein a shape

of the first device region is different from that of the second device region.

15. The semiconductor device of claim 3, wherein a channel region of the first or second conductivity type transistor is formed in a plane perpendicular to a substrate surface.

16. The semiconductor device of claim 15, wherein a direction of an electric current flowing through the channel region of the first or second conductivity type transistor is horizontal to the substrate surface.

17. The semiconductor device of claim 3, wherein the first or second device region includes a Fin structure including a plurality of rectangular strips.

18. The semiconductor device of claim 17, wherein, in the semiconductor device, a plurality of channel regions are formed in perpendicular to a substrate surface, a direction of an electric current is horizontal to the substrate surface, and the channel regions are completely depleted during operation.

19. The semiconductor device of claim 18, wherein a ratio of a number of Fins of the channel of an n-type transistor to a number of Fins of the channel of a p-type transistor of the semiconductor device is 1.0 or more and 2.0 or less.

20. A manufacturing method of a semiconductor device, comprising:

depositing a hard mask material on a gate electrode

material;

forming a dummy gate pattern on the deposited hard mask material;

depositing a material for forming a sidewall around the dummy gate pattern;

etching the material for forming the sidewall while the sidewall is left;

selectively removing the dummy gate pattern;

depositing resist, by lithography, to form a region coupling a gate electrode with a metal wiring;

processing a hard mask of a gate electrode region;

removing the resist; and

processing the gate electrode region using the hard mask.